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HARMONIC ANALYSIS OF MULTILEVEL INVERTER

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ABSTRACT

This paper present the different levels of cascaded H-bridge inverters and the minimization of total harmonic distortion by increasing levels. Selective Harmonic Elimination technique is used as a switching scheme. The analysis of three, five and seven level cascaded H-bridge inverter simulation work is done by using the MATLAB software and experimental results have been presented to validate the theory. The simulation results show the improvement of output voltage waveform and reduction of the THD by increasing the levels in inverter.

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KEYWORDS: Cascaded Multilevel Inverter, selective harmonic elimination, etc.

INTRODUCTION

Multilevel inverters have ability to generate low switching frequency high quality output waveforms with several high voltages and higher power applications. The general structure of the multilevel converter is to synthesize a sinusoidal voltage from several level of voltages [1][2]. The multilevel inverter has overcome the limitations of conventional two level voltage converters. The advantages of multilevel inverter are higher power quality, lower switching losses, low electromagnetic interference and higher voltage capability. There are mainly three types of multilevel inverter topologies used- (1) Diode clamp multilevel inverter (DCMI),(2) Flying capacitor multilevel inverter(FCMI) and (3) Cascade multilevel inverter (CHB)[3].Harmonic problems in multilevel inverter is the most important one with distress the output voltage and increased level of switching strategy.

There are numerous methods like (SPWM) Sinusoidal Pulse Width Modulation, (MCPWM) Multi-Carrier Pulse Width Modulation and (SHE-PWM) Selective Harmonic Elimination Pulse Width Modulation are implemented for harmonic elimination in multilevel inverter. (MCPWM)Multi-Carrier Pulse Width Modulation strategies is widely used, because it can be easily implemented to low voltage modules. Normally MCPWM can be categorized as Level Shifted PWM (LS-PWM) and Phase Shifted PWM (PS-PWM) methods.(LS-PWM) Level Shifted PWM is characterized into three i.e. Phase Disposition Technique (PD) ,Phase Opposition Disposition Technique (POD) and Alternative Phase Opposition Disposition Technique (APOD).

For systems where high switching efficiency is needed, it is desirable to keep the switching frequency much lower. In this state, another approach is to choose the switching angle in such a way that a desired fundamental output is generated and chosen harmonics of the fundamental voltage are suppressed, this is called as harmonic elimination or programmed harmonic elimination to eliminate specific harmonics[4]. The characteristic of the SHE-PWM method is that the waveform analysis is performed by using Fourier theory. The sets of non-linear transcendental equations are derived, and the solution is obtained by using an iterative method.

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CASCADED H-BRIDGE INVERTER

Cascaded multilevel inverter is the most important topology in inverter family because of several multiple configurations. CHB is a combination of several series connected H-bridge inverter having equal DC source in Fig.1. The circuit layout of CHB is easier then DCMI and FCMI. In CHB multilevel inverter, each level is having the same structure and there is no extra clamping diode or voltage balancing capacitor. For five H-bridge inverter

and each H-bridge uses IGBT (Insulated Gate Bipolar Transistor) switches it has more features than the other power semiconductor devices.

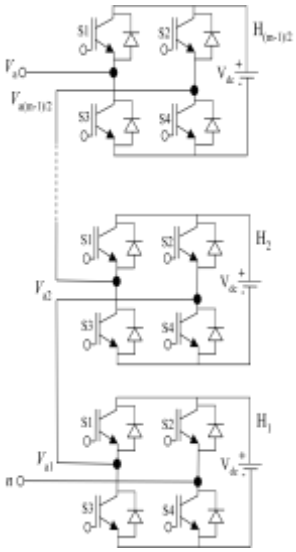

Fig.1 Single-phase cascade multilevel inverter

The traditional inverter does not eliminate completely the unwanted harmonics from output waveform. Therefore, by using multilevel inverter as an alternative to traditional PWM inverters is investigated. AC output voltage of different level,each full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

Cascaded H-bridge multilevel inverters mostly use IGBT switches. These switches have low block voltage and high switching frequency handle higher amount of power. CHB multilevel inverter initiate the idea of Separate DC Sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source i.e. Vdc. By cascading the AC outputs of each H-bridge, an AC voltage waveform is generated. The circuit layout of CHB is easier then DCMI and FCMI. In CHB multilevel inverter, each level is having the same structure and there is no extra clamping diode or voltage balancing capacitor. The number of switches can be easily reduced by using the new topology [6][7][8].

METHODOLOGY

Basic Principle

In CHB the number of output voltage level is defined by 2n+1, where n is the number of dc sources. . In this type of inverter, each cell has separate dc source, so each power circuit needs just one dc voltage source. The number of dc sources are proportional to the number of phase voltage levels .Each H-bridge cell having (positive) +Vdc, (negative)-Vdc and (zero) 0 output voltages. The phase output voltage is synthesized by the sum of four inverter outputs,i.e., $v_{an} = v_1 + v_2 + v_3 + v_4$. This is made possible by connecting the dc sources sequentially to the ac side via the four gate-tum-off devices.

Each level of the full-bridge converter consists of four switches, S_1, S_2, S_3 and S_4. The ac output voltage at each level can be obtained by the appropriate switching manner. Minimum harmonic distortion can be obtained by controlling the cortducting angles at different inverter levels

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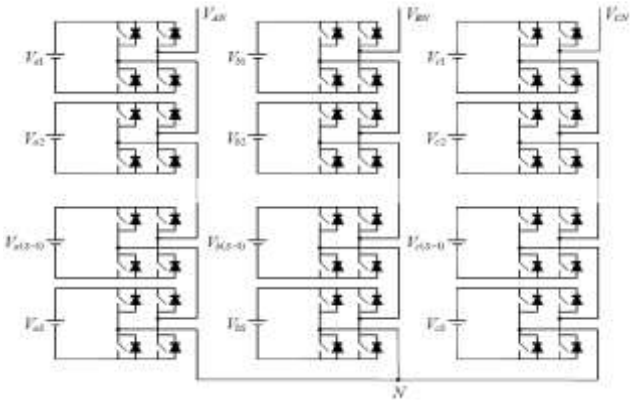

Fig.2 A general three-phase Wye-configuration cascaded-inverter

For a three-phase system, the output voltage of three cascaded inverters can be connected in two configuration wye or delta. For example, a wye configured m-level cascaded inverter with s separate capacitor is illustrated in Fig 2

Features

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. The structure of separate dc sources is well suited for various renewable
energy sources such as fuel cell, photovoltaic, and biomass,
etc.Connecting separated dc sources between two converters
in a back-to-back fashion is not possible because a short circuit will be introduced when two back-to-back converters
are not switching synchronously.

The major advantages of the cascaded inverter can be summarizes as follows:

- Compared with the diode-clamped and flying-capacitor inverter, it requires the less number of components to achieve the same number of voltage levels.
- Optimized circuit layout and packaging is possible because each level is having same structure and there are no extra clamping diodes or voltage –balancing capacitors.
- Soft-switching techniques can be used to reduce switching losses and device stresses.

The major disadvantages of the cascaded inverter can be summarized as follows:

- It needs separate dc sources for real power conversations, thereby limiting its applications.
- Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.

RESULTS AND DISCUSSION

All simulation results of the proposed converter for three-level, five-level and seven-level are done on MATLAB/Simulink. The simulation results are discussed for single phase five-level inverter with separate equal DC sources. The simulation is carried out in following three cases.

CASE- 1 In this case we will find out voltage and THD for three-level CHB inverter. The simulation diagram and corresponding waveforms are showm in fig.2.

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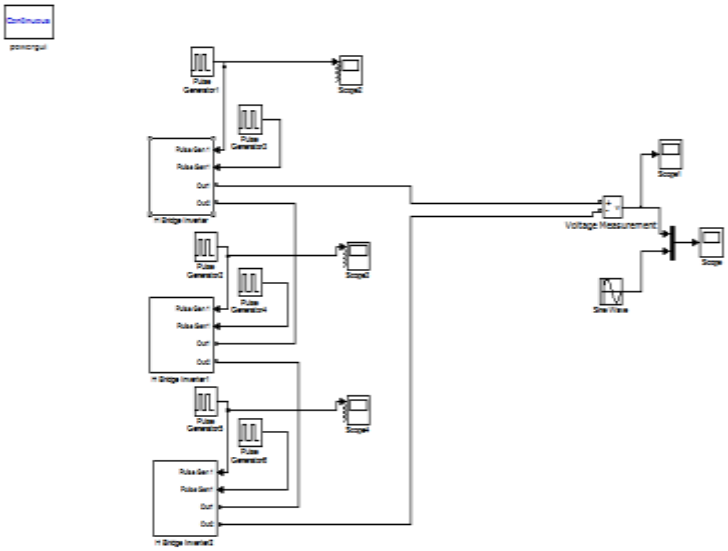

Fig.3 Simulink model of single-phase Three-level Inverter

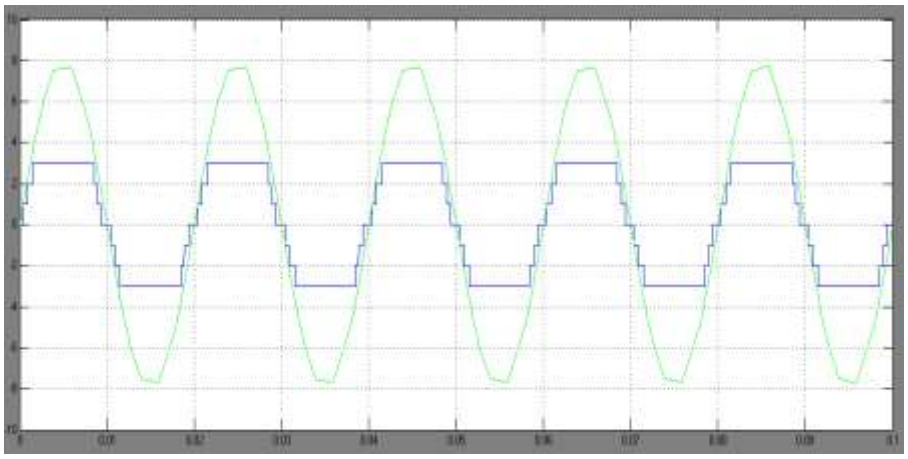

Fig.4 Simulation result of three-level inverter

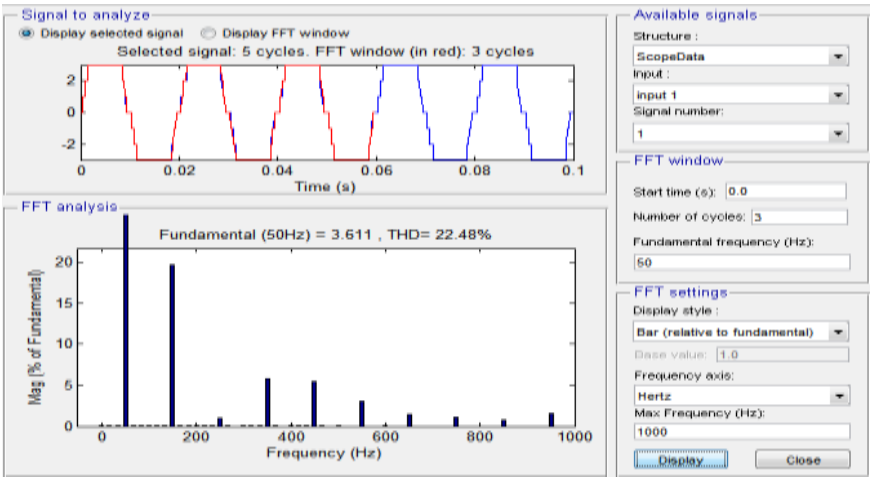

Fig.5 FFT Analysis of three-level H-bridge MLI

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CASE-2 In this case we will find out voltage and THD for five-level CHB inverter. The simulation diagram and corresponding waveforms are showm in fig.2.

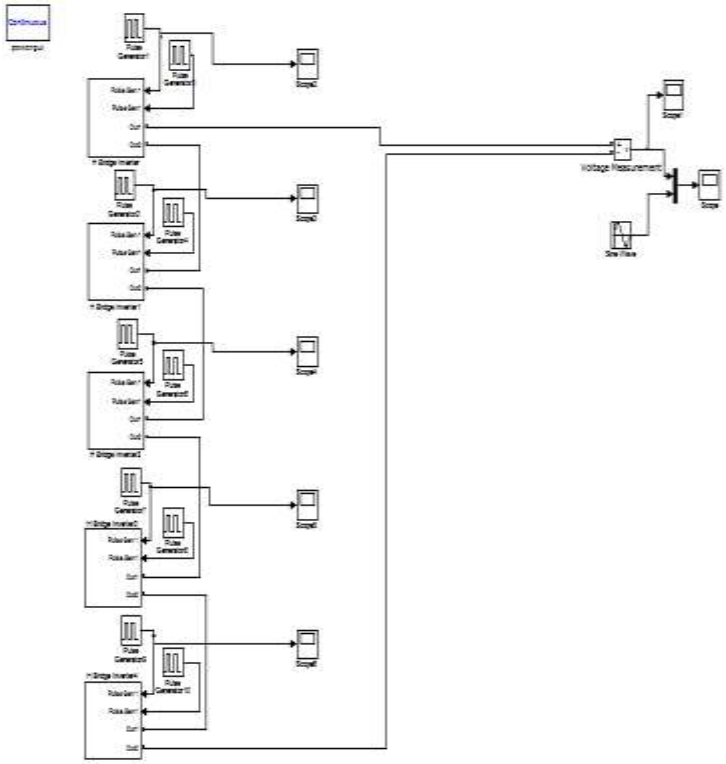

Fig.6 Simulink model of single- phase Five-level Inverter

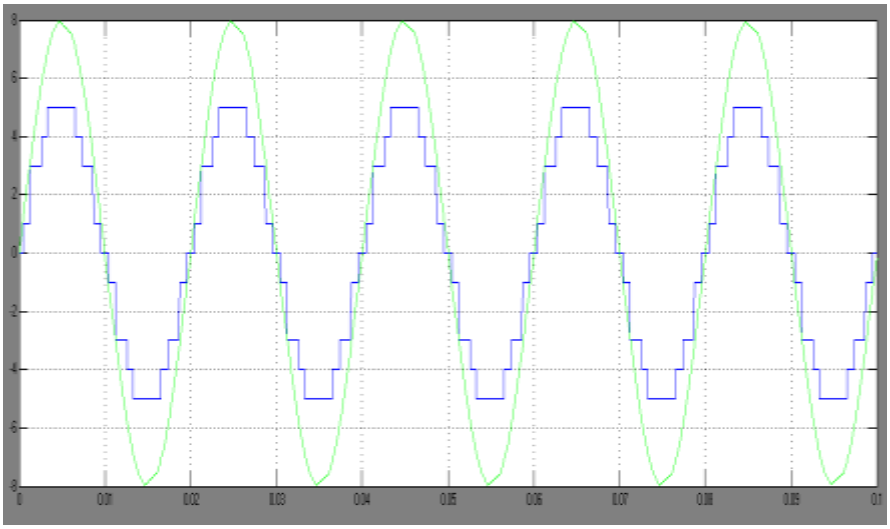

Fig.7 Simulation result of Five-level Inverter

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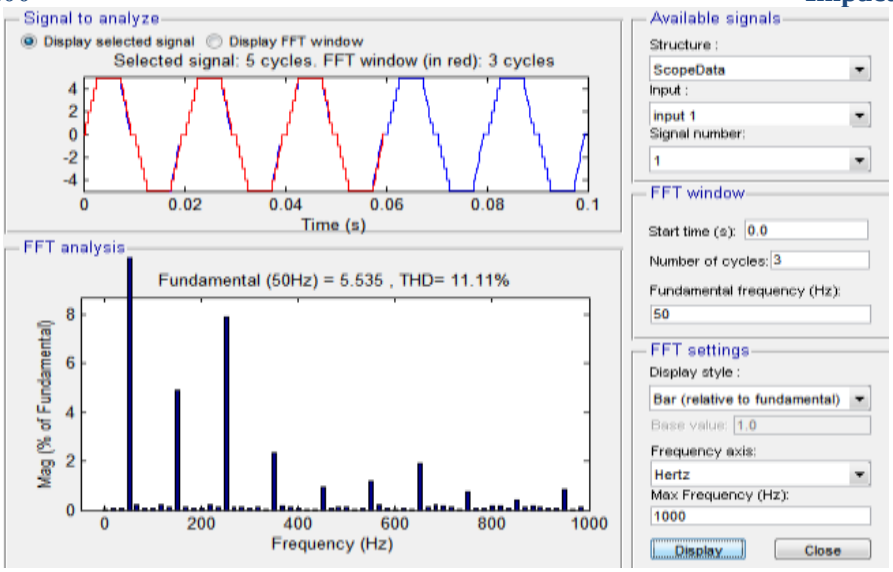

Fig.8 FFT Analysis of five-level H-bridge MLI

CASE-3 In this case we will find out voltage and THD for seven-level CHB inverter. The simulation diagram and corresponding waveforms are showm in fig.2.

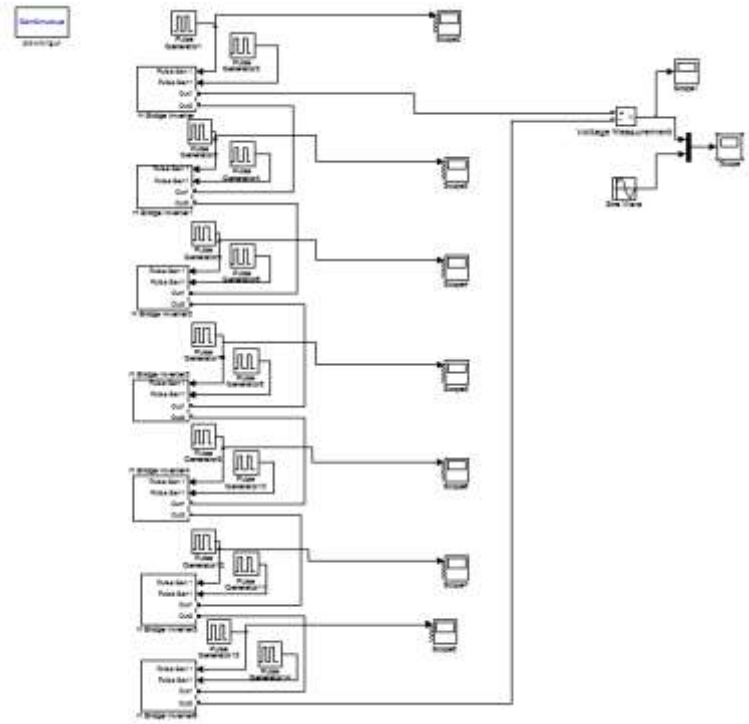

Fig.8 Simulink model of single –phase Seven-level inverter

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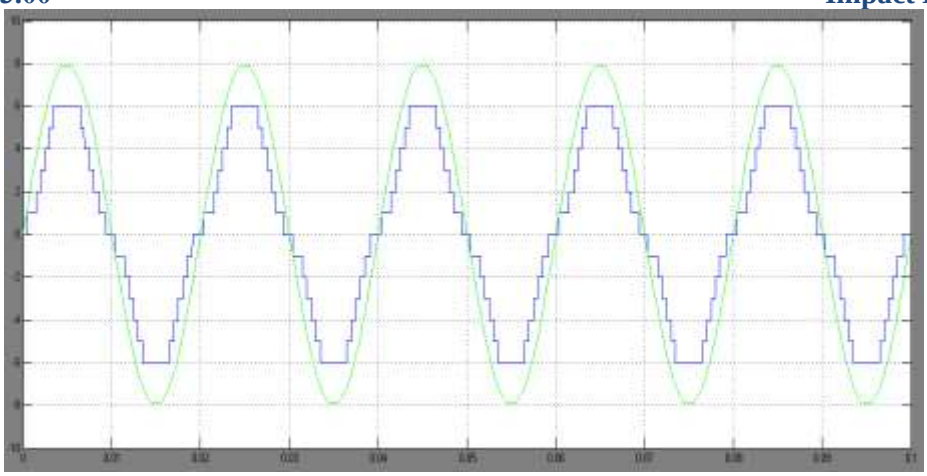

Fig.9 Simulation result of seven-level inverter

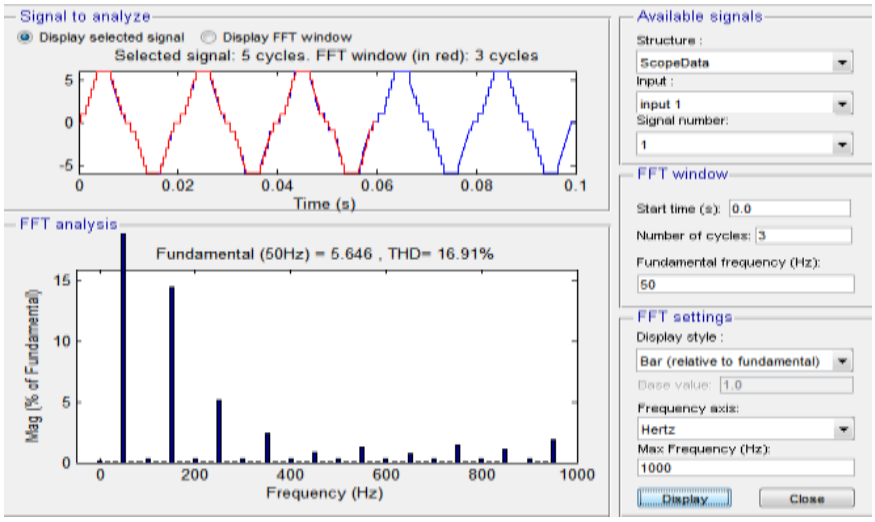

Fig.10 FFT Analysis of seven-level H-bridge MLI

Table. 1 Performance of THD level

LEVELS	%THD
3	22.48
5	11.11
7	16.91

CONCLUSION

The simulation of the three-level, five-level and seven-level inverter is successfully done using Selective Harmonic Elimination pulse width modulation technique. In this paper a three inverters with different levels has been designed and compared their THDs. From the comparison we identify that as level of the inverter is increases the Total Harmonic Distortion is decreases and the performance is improved. For analysis of this inverter SHE (Selective Harmonic Elimination) method can also be used to reduce harmonics.

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